07-24-06 PART B - FEE(S) TRANSMITTAL

140		PART I	3 - FEE(S) TRAN	SMIT	TAL				
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JUL 2.1 2006 3	<u>u</u> y)		or <u>Fax</u>	Alexan (571)-2	iaria, vi 273-2885	rginia 2	2313-1450		
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D1 FC:1501 1400.00 DA					Contre Coll Calillo (Signature)				
	00.00 DA		<u> </u>	Jul	<u> </u>	2006		(Date)	
APPLICATION NO.	FILING DATE		FIRST NAMED INVEN				RNEY DOCKET NO.	CONFIRMATION NO.	
10/697,357 10/29/2003 Viswanathan Lakshmanan 03-1772 81610 7491 FITLE OF INVENTION: METHOD OF PARTITIONING AN INTEGRATED CIRCUIT DESIGN FOR PHYSICAL DESIGN VERIFICATION									
APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE D	JE PRE	EV. PAID IS	SUE FEE	TOTAL FEE(S) DUE	DATE DUE	
nonprovisional	NO	\$1400	\$300		\$0		\$1700	10/10/2006	
EXAM	IINER	ART UNIT	CLASS-SUBCLASS						
DOAN, N	716-007000								
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LSI Logic Corporation Milpitas, California									
Please check the appropr	riate assignee category or	categories (will not be p	rinted on the patent):	☐ Indi	vidual 🔯	Corporati	on or other private grou	p entity Government	
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